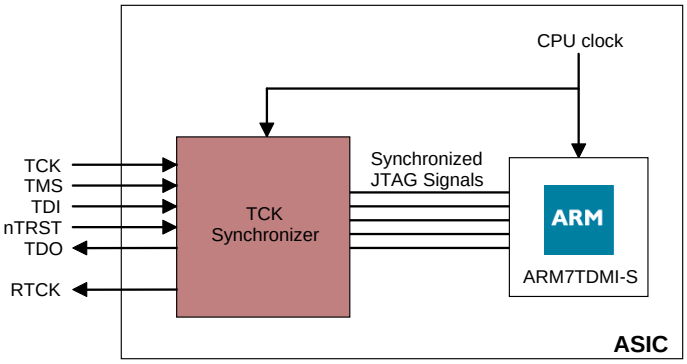
Turbo TCK Synchronizer ™

High speed JTAG synchronizer for synthesizable ARM cores

Turbocharged ARM test and debug performance



A TCK synchronizer is required to interface synthesizable ARM cores to standard JTAG compliant products such as ICEs and production test equipment.

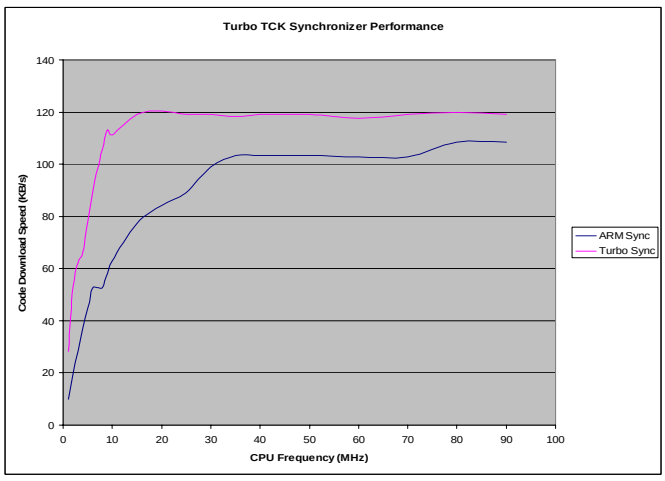
The following ARM cores are synthesizable. It is likely that all future ARM cores will also be synthesizable. They are delivered as VHDL or Verilog and designated by a '-S' at the end of the part number:

- **ARM7TDMI-S**
- **ARM926EJ-S, ARM946E-S, ARM966E-S, ARM968E-S**
- **ARM1026EJ-S**
- **ARM1136J-S, ARM1136JF-S, ARM1156T2-S, ARM1156T2F-S, ARM1176JZ-S, ARM1176JZF-S**

All synthesizable ARM cores are rising edge clocked throughout and provide debug access via JTAG. However the JTAG standard requires that the JTAG signals are synchronized to TCK and that TDO is generated on the falling edge of TCK.

Therefore ARM publish a TCK synchronizer circuit which can be used to interface IEEE standard JTAG with a core operating in a single clock rising edge domain - see diagram above.

However the standard ARM design has a significant performance impact at low CPU clock speeds (<100MHz) – see graph below.



Many modern microprocessors such as the popular ARM family use the industry standard IEEE 1149.1 JTAG boundary scan system for device test and access to on-chip debug hardware.

However synthesizable ARM cores require an on-chip 'TCK synchronizer' circuit to be compatible with standard JTAG compliant products such as ICEs and production test equipment. This can reduce the JTAG performance.

The Turbo TCK Synchronizer from Debug Innovations is a replacement for the standard ARM design. It provides all the same signals to the core and the ICE except it requires only 2 CPU clocks per TCK transaction instead of 6, resulting in a 3x improvement in JTAG performance. The advantages are:

- **Improved production test performance (test times can be reduced by a factor of 3)**
- **Reduced Flash programming time**
- **Reduced test and programming costs**
- **Improved simulation performance for JTAG / debug**
- **Improved debug performance**
- **Enhanced engineering productivity**

The Turbo TCK Synchronizer also presents RTCK to the ICE earlier than the standard ARM design resulting in improved ICE performance.

No changes are required to the ARM core or application specific parts of your design. Just replace the standard ARM synchronizer block with the Debug Innovations' Turbo TCK synchronizer block. The functionality will be identical but the performance will be increased for simulation, debug, device testing and programming.

High speed replacement for ARM standard design

- 3 times the JTAG performance
- Identical signals to ARM standard design
- TCKEN is still 1 CPU clock wide
- Generates RTCK for the ICE / ATE
- TDOen supported
- Can be used with chained TAP controllers / multi-processor designs

Easy to integrate

- 100% synthesizable logic
- Similar gate count to ARM standard design
- Shipped with comprehensive testbench
- Includes ARM standard design as reference
- Designed by world renowned debug authority (the designer of ARM's best selling Multi-ICE)

Turbo TCK Synchronizer is available as licensable IP. Contact sales@debuginnovations.com for more information.

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Debug Innovations Ltd
16 Moat Way,
Swavesey,
Cambridge
CB4 5TR
United Kingdom

info@debuginnovations.com
www.debuginnovations.com

Tel: +44 1954 203080
Fax: +44 1954 200255

debug innovations 0101001101